

A Low-Volume, Low-Mass, Low-Power UHF Proximity Micro-Transceiver for Mars Exploration

William Kuhn¹, Norman Lay², Edwin Grigorian²

wkuhn@ksu.edu, norman.e.lay@jpl.nasa.gov, edwin.r.grigorian@jpl.nasa.gov

¹Kansas State University

²Jet Propulsion Laboratory, California Institute of Technology

Abstract—A UHF half-duplex micro-transceiver measuring 1 cm³, weighing less than 10 grams, and operating at 40 mW on receive and 50mW, 300mW, or 3W on transmit is described. The micro-transceiver is being designed for future Mars exploration missions, but can be adapted for other proximity links. It supports transmission rates up to 256 kbps and higher in BPSK or QPSK format for data return and receives command/control instructions at up to 8 kbps. In addition to its low mass/power features, temperature compensated circuit and system design and radiation tolerance allow operation outside of large shielded enclosures, further reducing the mass and complexity of exploration vehicles.

I. INTRODUCTION

During the early decades of the twenty-first century, a stream of robotic missions will be launched to support the exploration of Mars. Miniaturized, lightweight, and low-power advanced telecommunications systems are among the needed technologies. Existing radio transceivers typically measure as large as 5000 cm³, weigh up to 5 kg, and consume more than 50 W on transmit and 10 W on receive. A transceiver measuring in the 1 cm³ range and operating at fractions of a Watt will enable the design of new types of Mars exploration craft ranging from low-cost, low-mass, networked ground sensors/rovers to airplanes or balloons. The micro-transceiver will communicate collected scientific results to earth by relaying data through Mars orbiters already under development as well as support surface-to-surface links for geographically extended local exploration.

The top-level design and specifications are described in this paper, with emphasis on the analog/RF integrated circuit portion of the micro-transceiver. The development effort targets operation in the Mars temperature and radiation environment using a rad-hard Silicon-on-Sapphire (SOS) IC process [1-2], and leverages recent advancements in on-chip power amplifier design techniques, resonant TR switch circuits, and the specific requirements of the Mars telecommunications environment. A companion paper [3] presents data on designing for the Mars environment temperature range of 25 C to -120 C. Measured data is presented in the companion paper for SOS active and passive

components as well as the Commercial Off-The-Shelf (COTS) components to be used in the implementation.

II. SYSTEM ARCHITECTURE

A top-level block diagram illustrating the micro-transceiver in relation to a host vehicle is shown in Figure 1. The transceiver interfaces to a microprocessor on-board a scout craft and transmits collected data to an orbiter using the Microtransceiver Electronics through a suitable external antenna (nominally a low-mass wire monopole or dipole).

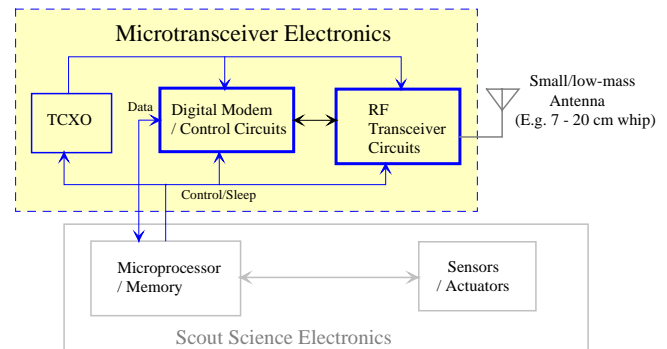


Figure 1. Top-level diagram of micro-transceiver and external interfaces.

Frequencies of operation and data formatting are a subset of those specified in the Proximity-1 Space Link Protocol recommendations [4]. The nominal uplink (micro-transceiver to Orbiter) frequency is 400 MHz, and the nominal downlink frequency is 440 MHz. Transmit power levels are selectable from 10 mW to 1 W to suit particular mission requirements. Data transmission is via suppressed or residual carrier BPSK modulation or via QPSK modulation at rates up to 256 kbps. Higher rates are supportable for local links [5]. The micro-transceiver also receives command and control data from the orbiter/relay. Command reception is limited to rates up to 8 kbps to reduce size and power consumption of digital circuits. Total power consumption on transmit can be as low as 50 mW and total power on receive can be reduced to less than 0.5 mW using a sleep mode conservation approach with a 1 % duty cycle.

A more detailed block diagram of the Micro-transceiver with internal interfaces shown is provided in Figure 2 and a mockup of what a final PCB could look like is shown in Figure 3. The transceiver consists of two primary integrated circuits (an RFIC and a digital IC) and an optional third IC for the 1 W output power option. Also included are a commercial temperature compensated crystal oscillator (TCXO) and IF filter, together with a small collection of surface mount passives providing required supply bypassing and optional antenna impedance-matching functions.

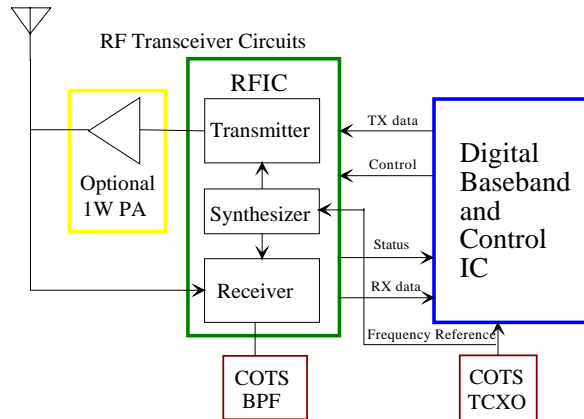


Figure 2. Simplified block diagram of micro-transceiver and internal interfaces.

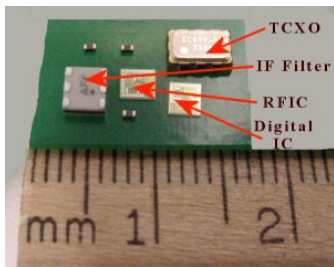


Figure 3. Physical mockup of full transceiver. 10/100mW version.

III. DESIGN TRADEOFFS

The micro-transceiver is designed for exploration vehicles which require very low-volume, low-mass, and low-power electronics. The goal is to provide a medium performance UHF relay solution that is interoperable with the existing communications infrastructure. However, it is important to note that the low-power/low-mass/low-volume feature is the overriding goal. To meet this goal, many modes of operation that may be present on more traditional transceivers are excluded in this design. For example, power output is low 10/100 mW (or 1 W maximum using optional PA integrated circuit), operation is limited to half-duplex, and signals to/from the transceiver are custom CMOS rather than more traditional RS-232/422 or other standard interconnects. In

addition, support for packet framing and link establishment/maintenance (e.g. ARQ) is limited within the transceiver itself.

In return for these limitations, the volume and mass of the transceiver are two to three orders of magnitude lower than that of the transceivers on-board the Spirit and Opportunity rovers, and the power consumption is one to two orders of magnitude less. This tradeoff favors application on very small and/or low mass vehicles such as micro-rovers, balloons, aerobots, and networked landers. To the extent possible, the microtransceiver is also designed to operate with low radiation shielding and minimal thermal insulation. All of these features contribute to final system solutions offering expanded exploration opportunities.

Finally, the design is partitioned into multiple die rather than targeting a “single-chip” solution. This decision was made to minimize development risk and to provide maximum flexibility. The multi-die decision has minimal impact on the overall mass/size/power goal while offering better paths for upgrading or retargeting to applications outside the Mars role for which it is being designed.

IV. RFIC ARCHITECTURE

The detailed architecture of the RFIC die is shown in Figure 4. For reliability and development risk-reduction, it employs relatively traditional direct-conversion transmitter and superheterodyne receiver architectures operated in a half-duplex mode. Both share a common UHF synthesizer which generates the necessary quadrature sinusoids needed for IQ modulation and for image-reject mixing. The synthesizer operating frequency, as well as most control functions of the IC, are programmed through a 3-wire serial bus with 3V CMOS logic levels.

A single synthesizer is feasible due to the half-duplex operating mode. This conserves power and die area and also allows the elimination of bulky duplex filters. In addition, it permits the co-location of power amplifier circuits on the same die as the sensitive receive circuits. During transmit, the synthesizer is programmed to the desired output frequency (e.g. 404.4 MHz) by the digital baseband/control IC. During receive, the synthesizer is programmed to the receive frequency (e.g. 435.6 MHz) plus the IF (nominally 10.7 MHz). This high-side injection strategy is used to provide better tracking of the TCXO and IF filter changes with temperature [3].

Within an application circuit, the system’s antenna is connected simultaneously to the RFIC’s LNA input and one of the PA outputs. During transmit mode, a reflective switch at the input to the LNA steers the transmit signal to the antenna and protects the LNA from the large voltages associated with 100 mW to 1 W operation (when using the optional external 1 W PA IC). During receive, the transmitter outputs become reflective terminations so that the majority of the receive signal power is routed to the LNA, minimizing noise figure. These reflective terminations are represented by

the open-circuit switches shown in Figure 4, although the actual implementations employ parallel-resonant tanks which are combined with impedance-matching circuits. Details of the resonant switch design can be found in reference [6].

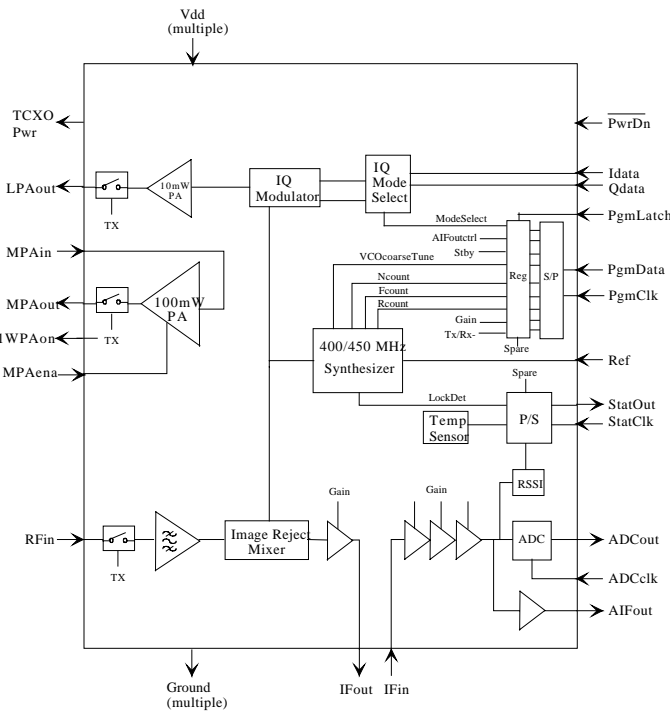


Figure 4. Transceiver RFIC block diagram

A. Receive-mode Operation

In receive mode, the switch in-line with the RFin signal of Figure 4 is closed and the signal encounters approximately 16 dB of gain in the tuned-RF LNA followed by approximately 20 dB of gain within the image-reject (IR) mixer. IR mixing is employed to minimize noise figure only. Actual image signal rejection is not a critical performance parameter within the Mars environment. Similarly, since the interference environment at Mars is more benign than that in terrestrial radio systems (e.g. cell phones) low input compression can be traded for low power operation. Further, to optimize noise figure performance, only limited filtering provided by the matching circuits is used in front of the LNA. These issues should be carefully considered by the system designer to guarantee electromagnetic compatibility with other electronics onboard the scout craft.

Following downconversion, the received signal is amplified at a 10.7 MHz intermediate frequency. The IF signal is routed off-chip to an IF filter which restricts the bandwidth to approximately 300 kHz. This bandwidth provides the spectrum narrowing required to prevent saturation of later stages of the IF amplifiers by broadband downconverted noise. In addition, it is needed to provide adequate prefiltering for 1-bit analog-to-digital conversion and subsequent demodulation functions in the digital modem/control IC.

The 1-bit ADC is clocked by an off-chip signal provided to it from the TCXO or the digital modem/control IC. The nominal clock frequency is specified as 19.200 MHz to prevent harmonics of the clock from interfering with receive signal frequencies and to allow for integer division to data clocks which conform to Proximity-1 recommended rates up to 256 kbps (division by 75). This clock will typically be the same signal as the synthesizer reference input, and provided by the TCXO. For applications which provide their own ADC functions, an un-digitized IF output is also provided.

The level of the IF signal entering either the on-chip or off-chip ADC circuits can be controlled through gain control bits shifted into the RFIC together with the synthesizer frequency-control bits. 12 bits are used to provide approximately 72 dB of gain control in approximately 6 dB steps. The external controller IC can monitor the level out of the IF chain through the receive signal-strength indicator (RSSI) circuit periodically to update the gains and form a digital AGC loop. The RSSI circuit provides 2 bits of resolution as a digital code shifted out of the RFIC using the StatClk signal. Additional bits shifted out with the RSSI code include an indication of die temperature and bits determining if the synthesizer is locked.

B. Transmit-mode Operation

Transmit mode is entered by programming the synthesizer for the desired frequency and then bringing pin Tx high. This signal enables one or both PA circuits depending on the state of MPAena and shuts down unneeded receive circuits to save power. The signal also controls internal power sequencing circuitry to provide needed spurious emission reduction and protection of the LNA.

Following assertion of Tx, the digital modem/control IC monitors TxOn which indicates when power sequencing is complete and a carrier is being transmitted. Once TxOn is asserted, data may be fed to the IQ modulator in either analog or digital form. Selection of analog or digital inputs to the IQ modulator is provided by a control bit in the programming data that accompanies the synthesizer frequency and receive gain-control bits.

C. Power Control

The transceiver contains internal power management circuits to provide for sleep-mode power conservation as well as near-complete power down of both itself and the TCXO. Nominal power consumption on receive is 40 mW. This can be reduced to less than 0.5 mW using a wake/sleep duty cycle of 1 %, and to proportionally lower consumption with lower duty cycles.

V. DIGITAL MODEM / CONTROL IC

The top-level architecture of the digital IC is shown in Figure 5. In transmit mode, this IC provides forward error

12th NASA Symposium on VLSI Design, Coeur d'Alene, Idaho, USA, Oct. 4-5, 2005

correction (FEC) compatible with Proximity-1 protocols, and optional packet framing functions. In receive mode, the IC handles the demodulation task as well as bit/frame synchronization. A DFT-based algorithm allows acquisition of BPSK or QPSK modulated signals over a +/- 50 kHz search range. This extended range is provided to address frequency drift of the TCXO at temperatures below its rated range [3] as well as aging and Doppler issues.

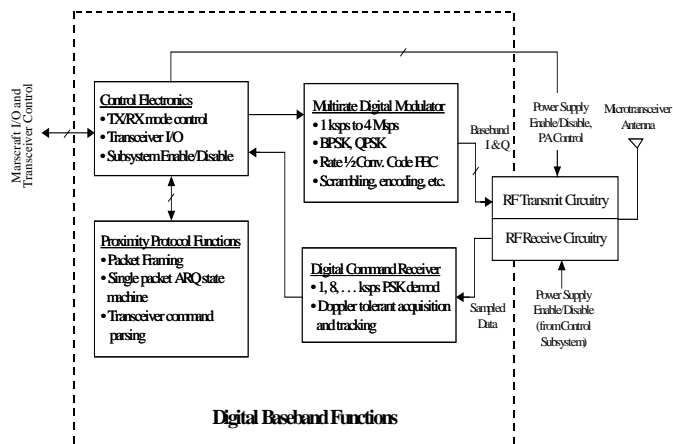


Figure 5. Digital Modem/Control IC functions.

Additional functions of the digital IC include control for the receiver and synthesizer circuits. At regular intervals, the IC monitors the RSSI output of the receiver and updates receiver gain settings to adjust for signal strength variations during an orbital pass. In addition, the VCO within the RFIC's synthesizer contains frequency range settings which are periodically monitored and updated to retain lock as IC or host PC-board temperatures vary.

VI. IC PROTOTYPING AND TEST

The custom RF circuits and digital signal processing algorithms discussed above are being developed at Kansas State University and the California Institute of Technology's Jet Propulsion Laboratory respectively, with oversight on circuit and IC process issues from Peregrine Semiconductor Corporation. To-date, initial prototyping of the receiver circuits within the RFIC and of the associated frequency acquisition, demodulation, and synchronization circuits has been completed. All circuits are being designed to work over the Mars temperature range of -100 to +25 C and to tolerate radiation exposure of up to 100 krad total dose.

A photograph of the first RFIC die, which includes all receiver circuits is shown in Figure 6. The synthesizer circuits are in the upper right quadrant. The LNA and RF switch functions are in the lower left quadrant, and the remainder of the receiver circuits are in the lower right. Test structures to allow for measurement and optimization of individual cells in future fabs are in the upper left.

A critical issue in a fully integrated receiver design is stability and crosstalk. Power to all circuitry is extensively filtered to prevent oscillation within the high-gain IF chain. In addition, multiple independent Vdd and grounds are provided in different parts of the circuits and whenever possible, circuitry is implemented in differential form.

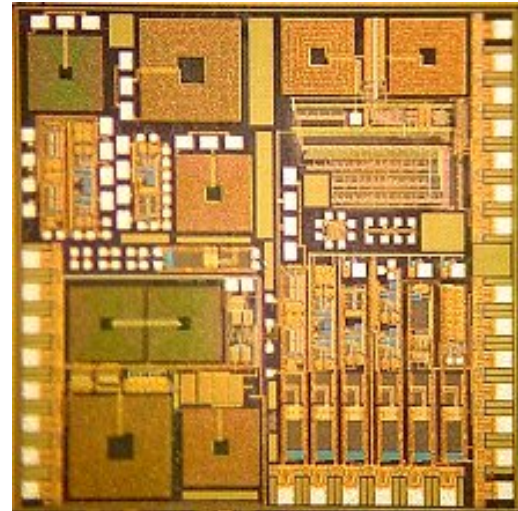


Figure 6. Die photograph of 1st spin receiver circuitry.

Initial testing, shown in Figures 7 and 8 indicates successful operation of all circuits, with some design centering and modifications needed within the tuned-RF amplifier circuits of the LNA. The measured noise figure of the LNA is approximately 3 dB, but the measured 8 dB gain is lower than expected due to inductor quality factor issues and slight mistuning in the output tank circuitry. These issues will be corrected in future prototyping runs. Overall, results are encouraging and suggest that the specifications in Table 1 should be met after minor revisions to circuits. Performance measurements over temperature will begin after a full PC board version of the test circuits is created.

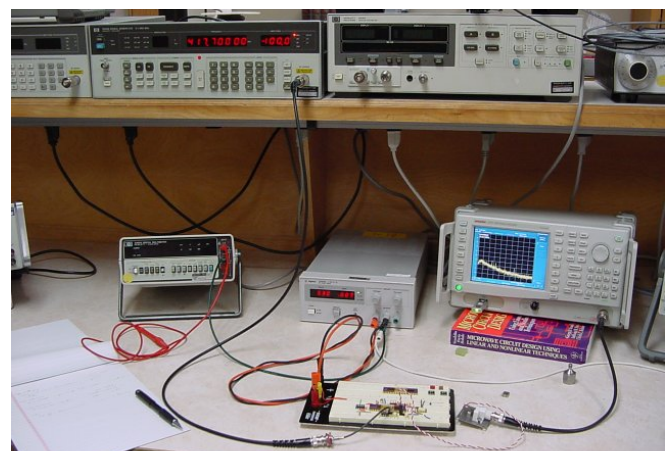


Figure 7. Early prototype testing.

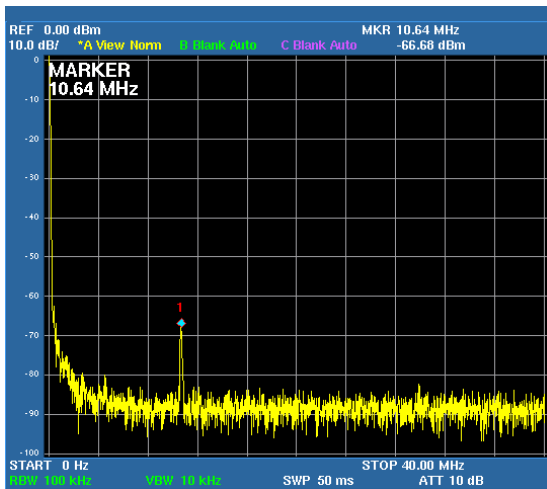
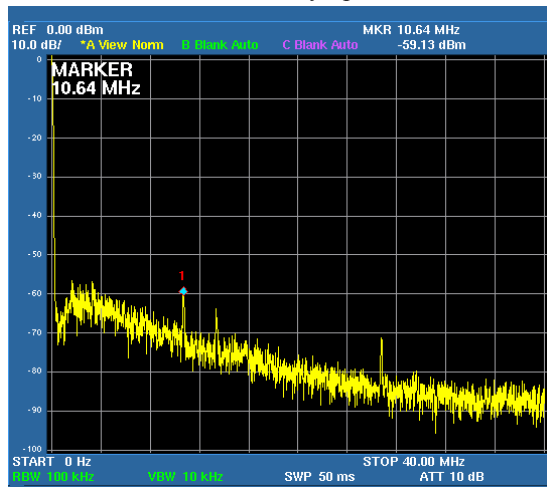


Figure 8. IF output before and immediately after IF filter.
(-100 dBm RF input, 100 kHz resolution bandwidth)

Table 1. Micro-transceiver Target Specifications

Parameter	Typ	Units
Power Supply Voltage	3.3	Volts
Power Consumption		
Transmit (10mW out)	50	mW
Transmit (100 mW out)	250	mW
Transmit (1 W out)	3	W
Receive (100% duty cycle)	40	mW
Tuning range		
Transmit	390 – 410	MHz
Receive	430 - 450	MHz
Tuning step size	< 100	kHz
TX frequency error		
-40 to +50C	< 10	ppm
-100 to -40C	< 150	ppm
Transmit bit rate	1 to 4096	ksps
Receive symbol rate	1 to 8	ksps
Receive sensitivity (1kbps)	-130	dBm

VII. SUMMARY AND CONCLUSIONS

A UHF micro-transceiver intended for future Mars scout missions and other space proximity links has been described. The goal is to provide a transceiver which is two to three orders of magnitude smaller, lighter, and lower-power than those currently available. While a number of tradeoffs have been made to achieve these goals, including limitation to half-duplex mode, reduced data rates, and support for a minimal subset of Proximity-1 protocols, the final transceiver should enable the development of new types of Mars exploration craft ranging from low-mass network ground sensors to airplanes and balloons. Results of prototyping to-date suggest that the target specifications for the micro-transceiver are reachable.

ACKNOWLEDGMENTS

This work was supported by the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration. The authors also gratefully acknowledge the work of the following individuals who have assisted in the design and layout process: Dan Nobbe, Yogesh Tugnawat, Igor Kuperman, Xin He, Mark Hartter, and Kai Wong.

REFERENCES

- [1] G. Lyons, "Commercial SOS technology for radiation-tolerant space applications," IEEE Radiation Effects Data Workshop, 24 July 1998, Page(s): 96 –99
- [2] R. Reedy, J. Cable, D. Kelly, M. Stuber, F. Wright, and G. Wu, "UTSi CMOS: A Complete RF SOI Solution", Technical Note at http://www.peregrine-semi.com/pdf_utsi_utsicmoscomplete.pdf
- [3] Y. Tugnawat and W. Kuhn, "Low temperature Performance of COTS Electronic Components for Future MARS Missions," University of Idaho 12th NASA Symposium on VLSI Design, Oct 4-5, 2005.
- [4] Proximity-1 Space Link Protocol Final Draft Recommendation for Space Data System Standards, CCSDS 211.0-R-3.2. Red Book. Issue 3.2. September 2002. <http://www.ccsds.org/rpa225/CCSDS-211.0-R-3.2.pdf>
- [5] N. Lay, C. Cheetham, H. Mojaradi, J. Neal, "Developing Low Power Transceiver Technologies for In Situ Communications Applications", *Interplanetary Networks Progress Report*, No. 42-147, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, November 15, 2001. http://ipnpr.jpl.nasa.gov/tmo/progress_report/42-147/title.htm.
- [6] W. B. Kuhn, M. Mojarradi, and A. Moussessian, "A resonant switch for LNA protection in watt-level CMOS transceivers," IEEE Transactions on Microwave Theory and Techniques, IEEEExplore, 2005 (To be published in print form later this year).